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10/735,899	12/16/2003	Atsuhiro Otaka	032172	5713

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EXAMINER	
TRUONG, LOAN	
ART UNIT	**PAPER NUMBER**
2114	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/735,899	OTAKA ET AL.	
	Examiner	Art Unit	
	LOAN TRUONG	2114	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 November 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3,5-11,13,15-19,21 and 23-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *7,27 and 28* is/are allowed.

6)☒ Claim(s) *1,3,5-6,8-11,13,15-19,21,23-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This Office action is in response to applicant's arguments on November 01, 2007.

2. Claims 1, 3, 5-11, 13, 15-19, 21 and 23-28 are presented for examination. Claims 2, 4, 12, 14, 20, 22 and 29-31 are cancelled.

Response to Arguments

3. Applicant's arguments filed November 01, 2007 have been fully considered but they are not persuasive.

In regard to claims 1, 11 and 19, applicant stated that Angelo failed to disclose the step of "*executing an update after a successful boot-up of said BIOS by writing to the memory in standby*" based on the fact that Angelo discloses updating the inactive half portion of memory and then a second boot-up occurs. As stated in the Office action mailed September 01, 2007, the term second boot-up can also be implied that there was a first preceded boot-up. Since the system cannot be booted with a defective/corrupted BIOS and upgrading requires writing to FLASH or NVRAM, it would be inherent that the first boot-up was successful *(col. 1 lines 47-62)*.

Secondly, applicant stated that Angelo failed to disclose "*the now active memory, formerly the inactive memory, is again switched to the inactive state.*" First of all, examiner interprets the claim language to read "a redundancy management method that uses one of a pair of memories. When one memory cannot be booted the system would switch to the BIOS in standby and when a successful boot-up is performed the system would allow execution of an update. Then after the update is successful, switching the

updated memory to standby to update the previously in operation memory." Switching therefore is done when one memory cannot be booted or after a successful boot-up by updating. For this limitation, Angelo does teach of updating the inactive half of the BIOS and bringing the newly updated to active state and updating the older version now in standby (*col. 1 lines 47-62).* Lin teaches the method of shadowing the other BIOS program to be used when the other BIOS program is found to be corrupted (*paragraph 0010).* Since the memories are interchangeable from active to inactive based on corrupted or updated states, it would be inherent that when active memory is corrupted the standby would take over to update the corrupted memory now in standby and execute until itself is corrupted, thereby switching back to standby to be updated.

Furthermore, applicant stated that Angelo cannot execute switching due to the fact that the two BIOS are mounted in a single memory. The claims provided no clear details on the method of switching from one BIOS to another, therefore, Angelo does in fact teaches the switching of BIOS by providing the active and inactive capabilities (*col. 1 lines 47-62).*

Additionally, applicant stated that Angelo failed to suggest "permitting switching said memory in standby to in operation when the update of said BIOS in said memory in said standby succeeded." Angelo does in fact teach this limitation by allowing overwritten of the inactive half of the BIOS first. When overwritten is done, switching is performed by bringing up the newly overwritten portion of the BIOS as being active.

For the above reasons, the rejections are maintained.

Allowable Subject Matter

4. Claims 7 and 27-28 are allowed.

The following is a statement of reasons for the indication of allowable subject matter: The examiner deems claims 7 and 27 as novel when read as a whole for the limitations of a redundancy management method for BIOS comprising the steps of: preventing execution of said switching when said hardware is started up for power recovery.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

5. Claims 1, 3, 5-6, 8-11, 13, 15-19, 21, and 23-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Angelo et al. (US 7,073,064) in further view of Lin (US 2002/0099974).

In regard to claim 1, Angelo et al. teach a redundancy manager method for BIOS, comprising the steps of:

Using one of a pair of memories (*two separately programmable portions, col. 1 lines 47-49)*, which respectively store the BIOS for setting hardware in an environment in which OS can use said hardware, for operation and the other standby (*each contain identical copies of the BIOS software with an active and inactive portion, col. 1 lines 48-52)*;

Executing an update after a successful boot-up of said BIOS by writing to said memory in standby (*to update the BIOS, the inactive half is overwritten first, col. 1 lines 50-54)*;

Permitting switching said memory in standby to in operation when the update of said BIOS in said memory in standby succeeded (*once the system is power cycled the second time, the system is brought up with the newly portion of the BIOS being active, the older BIOS routine can be updated while it is inactive, col. 1 lines 52-56)*; and

Writing the BIOS of said memory switched to operation, to said memory switched to standby for redundancy after said switching (*the older BIOS routine can be updated while it is inactive, col. 1 lines 52-56*).

Angelo et al. does not teach the method for BIOS comprising the steps of switching to the BIOS in said memory in standby when the BIOS in said one memory cannot be booted;

Lin teaches the dual basic input/output system for a computer by assuming that the primary BIOS program is corrupted by not receiving the confirmation signal and shadow the secondary BIOS program into the predetermined CPU address space (*fig. 2, 107, paragraph 0029).*

It would have been obvious to modify the method of Angelo et al. by adding Lin dual basic input/output system for a computer. A person of ordinary skill in the art at the time of applicant's invention would have been motivated to make the modification because it would provide a robust integrity-checking feature of the BIOS program (*paragraph 0010).*

In regard to claim 3, Angelo et al. does not teach the redundancy management method according to claim 1, further comprising a step of switching said permitted memory in standby to in operation, and said memory in operation to in standby when said hardware is started up.

Lin teaches the dual basic input/output system for a computer by setting te GPI02 register to a value that will place a value on the selection signal line indicates usage of the secondary BIOS program (*fig. 3, 206, paragraph 0038).*

Refer to claim 1 for motivational statement.

In regard to claim 5, Angelo et al. does not teach the redundancy management method for BIOS according to claim 1, further comprising a step of preventing switching of said memory in

standby to said memory in operation when the update of said BIOS in said memory in standby failed.

Lin teaches the dual basic input/output system for a computer when the secondary BIOS program has not passed the checksum verification test the primary BIOS program must continue to be used *(fig. 3, 205, paragraph 0037)*.

Refer to claim 1 for motivational statement.

In regard to claim 6, Angelo et al. does not teach the redundancy management method for BIOS according to claim 1, further comprising a step of preventing switching said memory switched to standby, to said memory in operation when writing of said BIOS in said memory switched to standby failed.

Lin teaches the dual basic input/output system for a computer when the secondary BIOS program has not passed the checksum verification test the primary BIOS program must continue to be used *(fig. 3, 205, paragraph 0037)*.

Refer to claim 1 for motivational statement.

In regard to claim 8, Angelo et al. does not teach the redundancy management method for BIOS according to claim 1, further comprising a step of preventing execution of said redundancy step when said hardware is started up for power recovery.

Lin teaches the dual basic input/output system for a computer where the secondary BIOS program may be overwritten by a copy of the functional primary BIOS in recovery operation (*paragraph 0050).*

Refer to claim 1 for motivational statement.

In regard to claim 9, Angelo et al. does not teach the redundancy management method for BIOS according to claim 1, further comprising a step of executing the update of BIOS in a memory in standby of another hardware connected with said hardware according to the update of the BIOS in said memory in standby of said hardware.

Lin teaches the dual basic input/output system for a computer where recovery of BIOS by overwritten the secondary BIOS with a copy of the functional primary BIOS (*paragraph 0050).*

Refer to claim 1 for motivational statement.

In regard to claim 10, Angelo et al. does not teach the redundancy management method for BIOS according to claim 1, further comprising a step of executing the synchronization processing of the BIOS with another hardware connected with said hardware.

Lin teaches the dual basic input/output system for a computer where pure copying operation performed to place an identical copy of the primary BIOS into secondary BIOS (*paragraph 0050).*

Refer to claim 1 for motivational statement.

In regard to claim 11, Angelo et al. disclosed a data processing apparatus, comprising:

a hardware including a CPU (*fig. 3, 200)*;

a pair of memories (*two separately programmable portions, col. 1 lines 47-49)* which respectively store a BIOS for setting said hardware in an environment in which OS can use said hardware (*each contain identical copies of the BIOS software with an active and inactive portion, col. 1 lines 48-52)*; and

wherein said CPU executes the update of said BIOS after a successful boot-up by writing to said memory in standby (*to update the BIOS, the inactive half is overwritten first, col. 1 lines 50-54)*;

wherein said service processor permits switching said memory in standby to said memory in operation when the update of said BIOS in said memory in standby succeeded (*once the system is power cycled the second time, the system is brought up with the newly portion of the BIOS being active, the older BIOS routine can be updated while it is inactive, col. 1 lines 52-56)*, and

wherein said CPU writes the BIOS of said memory switched to operation, to said memory switched to standby for redundancy after said switching (*the older BIOS routine can be updated while it is inactive, col. 1 lines 52-56*).

Angelo et al. does not teach a data processing apparatus, comprising of a service processor for using one of said pair of memories for operation and the other for standby when said hardware is started up and switching to the BIOS in said memory in standby when the BIOS of said one memory cannot be booted.

Lin teaches the dual basic input/output system for a computer by assuming that the primary BIOS program is corrupted by not receiving the confirmation signal and shadow the secondary BIOS program into the predetermined CPU address space *(fig. 2, 107, paragraph 0029)*.

Refer to claim 1 for motivational statement.

In regard to claim 13, Angelo et al. does not teach the data processing apparatus according to claim 12, wherein said service processor switches said permitted memory in standby to a memory in operation, and said memory in operation to said memory in standby when said hardware is started up.

Lin teaches the dual basic input/output system for a computer where the primary BIOS has detected internal errors and BIOS switching circuit shadow in the secondary BIOS program *(paragraph 0034)*.

Refer to claim 1 for motivational statement.

In regard to claim 15, Angelo et al. does not teach the data processing apparatus according to claim 11, wherein said CPU prevents switching said memory in standby to the memory in operation when the update of said BIOS in said memory in standby failed.

Lin teaches the dual basic input/output system for a computer when the secondary BIOS program has not passed the checksum verification test then primary BIOS program must continue to be used *(fig. 3, 205, paragraph 0037)*.

Refer to claim 1 for motivational statement.

In regard to claim 16, Angelo et al. does not teach the data processing apparatus according to claim 11, wherein said CPU prevents switching said memory switched to standby, to said memory in operation when writing of said BIOS in said memory switched to standby failed.

Lin teaches the dual basic input/output system for a computer when the secondary BIOS program has not passed the checksum verification test then primary BIOS program must continue to be used *(fig. 3, 205, paragraph 0037)*.

Refer to claim 1 for motivational statement.

In regard to claim 17, Angelo et al. does not teach the data processing apparatus according to claim 11, further comprising another hardware connected with said hardware, and said hardware executes the update of the BIOS in the memory in standby of said other hardware connected with said hardware according to the update of the BIOS in said memory in standby of said hardware.

Lin teaches the dual basic input/output system for a computer where the recovery of BIOS by overwritten the secondary BIOS with a copy of the functional primary BIOS *(paragraph 0050)*.

Refer to claim 1 for motivational statement.

In regard to claim 18, Angelo et al. teach the data processing apparatus according to claim 11, wherein said hardware executes the synchronization processing of the BIOS with said other hardware connected with said hardware.

Lin teaches the dual basic input/output system for a computer where the pure copying operation performed to place an identical copy of the primary BIOS into secondary BIOS *(paragraph 0050)*.

Refer to claim 1 for motivational statement.

In regard to claim 19, Angelo et al. teach a storage system, comprising: a storage control apparatus comprises:

a hardware including a CPU *(fig. 3, 200)*;

a pair of memories *(two separately programmable portions, col. 1 lines 47-49)* which respectively store a BIOS for setting said hardware in an environment in which OS can use said hardware *(each contain identical copies of the BIOS software with an active and inactive portion, col. 1 lines 48-52)*; and

wherein said CPU of said storage control apparatus executes the update of said BIOS after a successful boot-up by writing to said memory in standby *(to update the BIOS, the inactive half is overwritten first, col. 1 lines 50-54)*;

wherein said service processor of said storage control apparatus permits the switching of said memory in standby to said memory in operation when the update of said BIOS in said memory in standby succeeded *(once the system is power cycled the*

second time, the system is brought up with the newly portion of the BIOS being active, the older BIOS routine can be updated while it is inactive, col. 1 lines 52-56), and

wherein said CPU of said storage control apparatus writes the BIOS of said memory switched to operation, to said memory switched to standby for redundancy after said switching (*the older BIOS routine can be updated while it is inactive, col. 1 lines 52-56*).

Angelo et al. does not teach a storage system comprising a service processor for using one of said pair of memories for operation and the other for standby (*Primary BIOS and Secondary BIOS, fig. 1A)* when said hardware is started up and switching to the BIOS in said memory in standby when the BIOS of said one memory cannot be booted (*Confirmation signal not received, then shadow secondary BIOS, fig. 2)*; and a plurality of storage devices (*flash ROM to hold primary and secondary BIOS program, paragraph 0031)* connected to said storage control device (*primary and secondary BIOS programs are executed by the CPU, paragraph 0011).*

Lin teaches the dual basic input/output system for a computer by assuming that the primary BIOS program is corrupted by not receiving the confirmation signal and shadow the secondary BIOS program into the predetermined CPU address space (*fig. 2, 107, paragraph 0029)* and the flash ROM are used to hold the primary and secondary BIOS program executed by the CPU (*paragraph 0011 and paragraph 0031).*

Refer to claim 1 for motivational statement.

In regard to claim 21, Angelo et al. does not teach the storage system according to claim 20, wherein said service processor of said storage control apparatus switches said permitted memory in standby to a memory in operation and said memory in operation to said memory in standby when said hardware is started up.

Lin teaches the dual basic input/output system for a computer where the primary BIOS program is corrupted, the computer system will automatically switch over to the secondary BIOS program (*paragraph 0030*) and the POST power-on-self-test allows primary BIOS program to test determine if it is functional (*paragraph 0031*).

Refer to claim 1 for motivational statement.

In regard to claim 23, Angelo et al. teach the storage system according to claim 19, wherein said CPU of said storage control apparatus prevents switching said memory in standby to the memory in operation when the update of said BIOS in said memory in standby failed.

Lin teaches the dual basic input/output system for a computer when the secondary BIOS program has not passed the checksum verification test then primary BIOS program must continue to be used *(fig. 3, 205, paragraph 0037)*.

Refer to claim 1 for motivational statement.

In regard to claim 24, Angelo et al. does not teach the storage system according to claim 19, wherein said CPU of said storage control apparatus prevents switching said memory

switched to standby, to said memory in operation, when writing of said BIOS in said memory switched to standby failed.

Lin teaches the dual basic input/output system for a computer when the secondary BIOS program has not passed the checksum verification test then primary BIOS program must continue to be used *(fig. 3, 205, paragraph 0037)*.

Refer to claim 1 for motivational statement.

In regard to claim 25, Angelo et al. teach the storage system according to claim 19, further comprising another storage control apparatus, which is connected to said storage devices and said storage control apparatus and for controlling said storage devices, wherein said storage control apparatus executes the update of the BIOS in the memory in standby of said other storage control apparatus according to the update of the BIOS in said memory in standby of said storage control apparatus.

Lin teaches the dual basic input/output system for a computer where the recovery of BIOS by overwritten the secondary BIOS with a copy of the functional primary BIOS *(paragraph 0050)*.

Refer to claim 1 for motivational statement.

In regard to claim 26, Angelo et al. teach the storage system according to claim 19, further comprising another storage control apparatus, which is connected to said storage devices and said storage control apparatus and for controlling said storage devices, wherein said storage

control apparatus executes the synchronization processing of the BIOS with said other storage control apparatus.

Lin teaches the dual basic input/output system for a computer where pure copying operation performed to place an identical copy of the primary BIOS into secondary BIOS *(paragraph 0050)*.

Refer to claim 1 for motivational statement.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. See PTO 892.

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to LOAN TRUONG whose telephone number is (571) 272-2572. The examiner can normally be reached on M-F from 8am-4pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, SCOTT BADERMAN can be reached on (571) 272-3644. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Loan Truong
Patent Examiner
Art Unit: 2114

SCOTT BADERMAN
SUPERVISORY PATENT EXAMINER